AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An electrostatic discharge protection device ~~is~~ located between a pad and an internal circuit, and ~~is~~ coupled between a first power wire and a second power wire, comprising:

a switching circuit for outputting an enable signal when receiving a detecting result signal;

~~a driving circuit coupled to the switching circuit for outputting a ground level signal when receiving the enable signal;~~

a voltage detecting device ~~including~~ comprising at least one serial diode connected between the first power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage level;

a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level;

a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third

predetermined voltage level lower than the second predetermined voltage level; ~~and~~

a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate ~~connected to the driving circuit and is turned on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the ground level signal~~; and

a driving circuit coupled to the switching circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

2. (Original) The electrostatic discharge protection device as claimed in claim 1, wherein the first switch and the third switch are NMOS transistors.

3. (Original) The electrostatic discharge protection device as claimed in claim 2, wherein the second switch is a PMOS transistor.

4-5. (Cancelled)

6. (Previously Presented) The electrostatic discharge protection device as claimed in claim 1, wherein the first power wire provides a power source signal.

7. (Previously Presented) The electrostatic discharge protection device as claimed in claim 1, wherein the voltage level of the second power wire is ground level.

8. (Original) The electrostatic discharge protection device as claimed in claim 7, wherein the second predetermined voltage level is a break down voltage of the NMOS transistor.

9. (Original) The electrostatic discharge protection device as claimed in claim 8, wherein the third predetermined voltage level is a voltage difference to make the PMOS transistor generate leakage current.

10. (Previously Presented) The electrostatic discharge protection device as claimed in claim 1, wherein the first controlling gate, the second controlling gate, and the third controlling gate are gates of MOS transistors.

11. (Currently Amended) An electrostatic discharge protection device located between a pad and an internal circuit, and ~~is~~

coupled to a first power wire, a second power wire, and a third power wire, comprising:

a switching circuit for outputting an enable signal when receiving a detecting result signal;

~~a driving circuit coupled to the switching circuit and the third power wire for outputting a ground level signal when receiving the enable signal;~~

a voltage detecting device ~~including~~ comprising at least one serial diode connected between the third power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the third power wire reaches a first predetermined voltage level;

a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level;

a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; ~~and~~

a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate ~~connected to the driving circuit and is turned on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the ground level signal~~; and

a driving circuit coupled to the switching circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

12. (Original) The electrostatic discharge protection device as claimed in claim 11, wherein the first switch and the third switch are NMOS transistors.

13. (Original) The electrostatic discharge protection device as claimed in claim 12, wherein the second switch is a PMOS transistor.

14. (Cancelled)

15. (Previously Presented) The electrostatic discharge protection device as claimed in claim 11, wherein the first power wire provides a first power source signal.

16. (Currently Amended) The electrostatic discharge protection device as claimed in claim 11, wherein the voltage level of the second power wire is in ground level.

17. (Original) The electrostatic discharge protection device as claimed in claim 16, wherein the second predetermined voltage level is a break down voltage of the NMOS transistor.

18. (Original) The electrostatic discharge protection device as claimed in claim 17, wherein the third predetermined voltage level is a voltage difference to make the PMOS transistor generate leakage current.

19. (Currently Amended) The electrostatic discharge protection device as claimed in claim 18, wherein the first controlling gate, the second controlling gate, and the third controlling gate are gates of MOS transistors.

20. (Previously Presented) The electrostatic discharge protection device as claimed in claim 11, wherein the voltage level

of the third power wire is transformed form the voltage level of the first power wire.

21. (New) The electrostatic discharge protection device as claimed in claim 1, wherein the enable signal output from the switching circuit is in ground level.

22. (New) The electrostatic discharge protection device as claimed in claim 11, wherein the enable signal output from the switching circuit is in ground level.